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Abstract

Integrated test circuit arrangement and test method

An explanation is given, inter alia, of a test circuit arrangement (10) containing both integrated test structures (T1 to T5) and an integrated heating element, an integrated supply unit (40) and integrated detection unit (42). Tests of a multiplicity of test structures (T1 to T5) can be implemented in a simple manner with the aid of this circuit arrangement (10).

(Figure 1)